Introduction to quantum science and technology

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Exercise 1 – Esaki Tunnel Diode

Consider the Esaki tunnel diode with the characteristic I-V of Fig. 1 with the high frequency equivalent circuit of Fig. 2, for a tunnel diode biased into the negative-resistance region.

a. Is the tunnel diode always a dissipative device or not (consider that it may have a region of differential negative resistance)? Is energy being dissipated in a process of direct band-to-band tunneling?
b. This device can be seen as a nonlinear resistor that is voltage controlled; the current I is a function of the voltage V. By virtue of the nonlinearity of the tunnel diode a network including the tunnel diode can have more solutions. Redraw the V-I characteristics (if the device would be operated at constant injected current) and highlight the negative resistance region.
c. Can this device be considered as an active amplifier in any of the operation regions?
d. Calculate the expressions of resistive cut-off frequency (frequency at which the real part becomes zero) for R_Q = - 20 Ω and R_S = 2 Ω, C = 0.1pF.

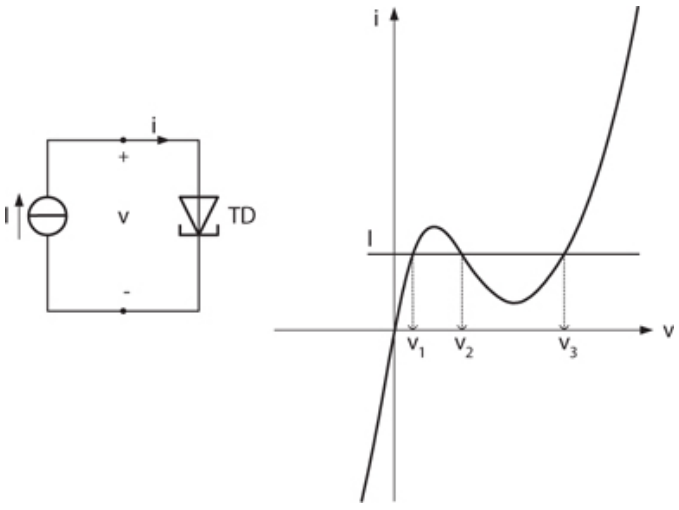

Figure 1 I-V characteristic of the Esaki tunnel diode

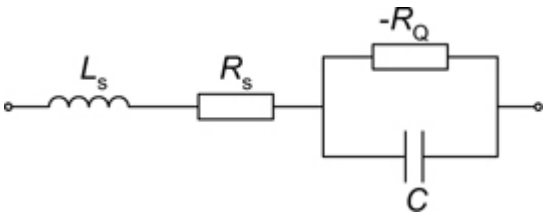

Figure 2 Equivalent circuit of the Esaki diode biased in the negative resistance region.

Solution Exercise 1:

a) As the I-V characteristic in Fig. 1 shows, the tunnel diode is a nonlinear resistor. A simple interpretation of this figure shows that the tunnel diode is a dissipating device; the instantaneous power entering the tunnel diode is always positive (although the differential resistance is sometimes negative). In a circuit the dissipated power is balanced by the power delivered by the source(s). In the case of band-to-band tunneling current and excess current, we may consider individual electrons because both currents involve the tunneling of single electrons; at sufficiently low-bias voltages the tunnel current can be described as composed of individual tunneling events that are uncorrelated.First consider the excess current. This excess current is mainly due to tunneling by way of energy states within the forbidden bandgap. In this type of tunneling, electrons start in the conduction band, tunnel to a single energy state or in steps to multiple energy states in the forbidden bandgap, and finally tunnel to an empty state in the valence band. Indirect tunneling in this way is a dissipative process.Now, secondly, consider the direct band-to-band tunneling. For small voltages, the I-V characteristics are reasonably well explained by assuming that electrons tunnel through the small barrier to empty states at the same energy level, causing the electron to follow a horizontal path in the energy band diagram. Actually, during this tunneling energy is conserved; so there is no energy dissipation during the tunnel event. However, according to the nonlinear I-V characteristic the device is dissipating; where is the energy? To solve this paradox, energy has to be dissipated outside the tunnel region.

b-c) Due to the nonlinear I-V characteristic we can call it a nonlinear resistor. This nonlinear resistor is voltage controlled; the current I is a (single-valued) function of the voltage V. By virtue of the nonlinearity of the tunnel diode a network including the tunnel diode can have more solutions. An example is shown in Fig.2: the inclusion of a capacitor (or junction capacitance) will change the circuit to a dynamic one having two stable points (v1, I) and (v3, I); the point (v2, I) is unstable. The resulting circuit can be switched between the two stable points.

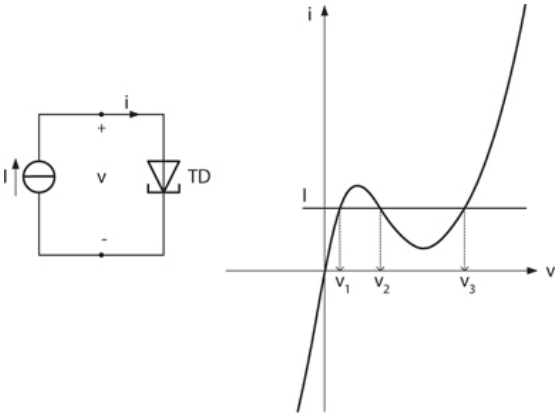

Figure 1 More solutions for a tunnel diode excited by an ideal current source.

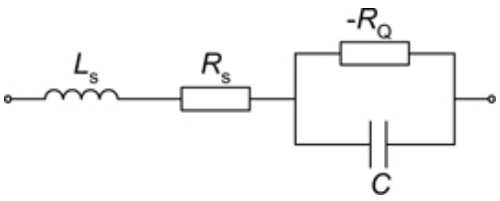

Figure 2 High-frequency equivalent circuit for a tunnel diode biased into the negative-resistance region.

The characteristic clearly shows the behaviour of the tunnel diode as a nonlinear passive resistance. Under small-signal conditions, however, the tunnel diode can be biased into a negative-resistance region in which the small signal or differential resistance $R_Q = dV/dI$, is negative. This makes the tunnel diode an active (linear) element in this region and power gain is available for small AC signals.

d) Now, the electronic behaviour of the tunnel junction can be examined by considering its equivalent circuit. The usual equivalent circuit consists of four elements: the series inductance L_s, the series

resistance R_s, the diode capacitance C, and the negative diode resistance $-R_Q$. Note the parallel combination of the diode capacitance and the tunnel resistance (biased in the negative-resistance bias). The impedance of the equivalent circuit is:

$$Z = \left[R_S - \frac{R_Q}{1 + \left(\omega R_Q C\right)^2}\right] + j\left[\omega L_S - \frac{\omega R_Q^2 C}{1 + \left(\omega R_Q C\right)^2}\right]$$

From Eq. 2.10 we can see that the resistive (real) part of the impedance will be zero at a certain frequency and the reactive part will be zero at a second frequency.

Generally, these frequencies are denoted as the **resistive cutoff frequency** fr and the **reactive cutoff frequency fr**, respectively. For the resistive cutoff frequency we obtain:

$$f_R = \frac{1}{2\pi R_Q C}\sqrt{\left(\frac{R_Q}{R_S}\right) - 1}$$

Exercice 2 Tunnel FET

The Tunnel FET is a gated p-i-n diode device operating in reversed bias regime and exploiting quantum-mechanical band-to-band tunneling. Select the correct properties of this steep slope device:

1. A **Tunnel FET with Germanium source** and a silicon Channel, having the same geometry and dimensions as an all-silicon Tunnel FET has a lower Ion current.
2. A **Tunnel FET with Germanium source** and a silicon Channel, having the same geometry and dimensions as an all-silicon Tunnel FET has a lower Ioff current.
3. **Trap-Assisted Tunneling (TAT)** is a phenomenon that does not depend on temperature but only on the energy levels of traps.

   False: TAT effect is removed at cryogenic temperatures (e.g. below 100K)
4. The **temperature dependence** trend of subthreshold characteristics of Tunnel FET is very similar to the one of MOSFETs made of same semiconductor material; the subthreshold slope degrades with the temperature increase.
5. **Carrier mobility** plays a key role in the transport characteristics of Tunnel FETs. Thus, materials with higher carrier mobility like III-V and Ge are suitable for these devices.
6. The **leakage current Ioff of Tunnel FETs** at cryogenic (sub-77K) temperatures is higher than at room temperature.
7. The **Electron-Hole Bilayer Tunnel FET** is a Density of States switch that can achieve a steeper transition between off and on than a conventional Tunnel FET because the gate-controlled electrostatic field and the tunneling paths are aligned.
8. Tunnel FET exploits a **discrete charge conduction principle** (electrons tunnel one by one from the conduction to the valence band).
9. The **steep-slope of Tunnel FETs** is normally steeper at lower levels of currents.
10. The output characteristics of Tunnel FETs saturate by carrier velocity saturation, as in case of nanometer scale MOSFETs.

Exercice 3 – Energetic considerations

How much energy is needed for one electron to tunnel onto a metallic island that has already n electrons and a total capacitance C_Σ to the ground?

Solution:

Figure 1 shows a small metallic initially electroneutral island embedded in an insulating medium. We can view the system as having a single capacitance C_Σ in which the island reflects one electrode of this capacitor and the environment forms the other electrode.

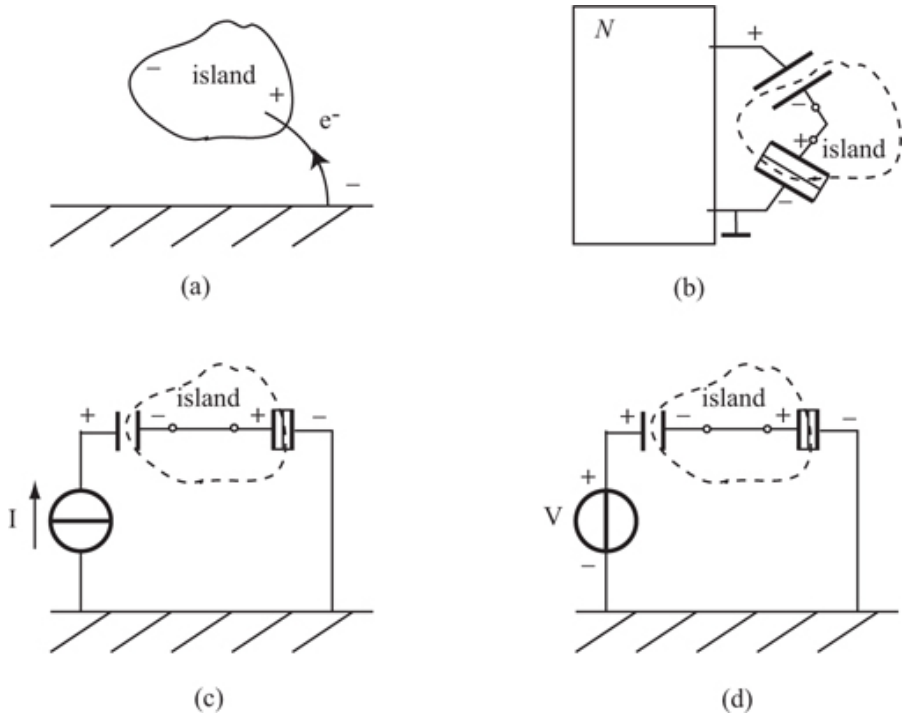

Figure 3 Tunneling of an electron toward an isolated island: (a) nonelectric energy source (b) energy source in electric network, N (c) energy provided by a current source (d) energy provided by an ideal voltage source.

The increase in energy when an electron is added to an island to which already n electrons have been tunneled is called the single-electron charging energy, $E_{ce}(n)$:

$$E_{CE}(n) = \frac{\big((n+1)e\big)^2}{2C_\Sigma} - \frac{(ne)^2}{2C_\Sigma} = \frac{e^2(2n+1)}{2C_\Sigma}$$

For initially uncharged islands the expression for the single-electron charging energy, Ece(n = 0), is called the Coulomb energy E_C:

$$E_C = e^2/2C_\Sigma$$

most texts on single-electron tunneling (SET) circuits interpret this Coulomb energy as the electrostatic energy barrier felt by the single electron moving onto or from an electrically neutral island. Tunneling is forbidden until this barrier can be surmounted when an energy source is applied that provides enough energy during tunneling. In this situation a Coulomb blockade exists if during tunneling not enough energy is supplied.

Exercice 4:

Propose and explain with a schematic and a discussion of the principle, how a Single Electron Transistor (SET) can be used for charge detection and exact quantification of the charge measured?

Solution:

A quite straightforward application of SETs is sensing charge at the gate capacitor. The working principle of this very sensitive electrometer is based on the offset of the I-V characteristic of the SET transistor as the charge on the gate capacitor changes to values larger than zero. Given the extremely high transconductance of the device, small charges (e.g., between 0 and e/2) of electrostatic potential at any of the controlling gates lead to measurable changes in the output current. Because of this, SETs are usually implemented to readout the occupation state of quantum dot hosting spin qubits (Fig. 4), where tunneling events must be monitored.

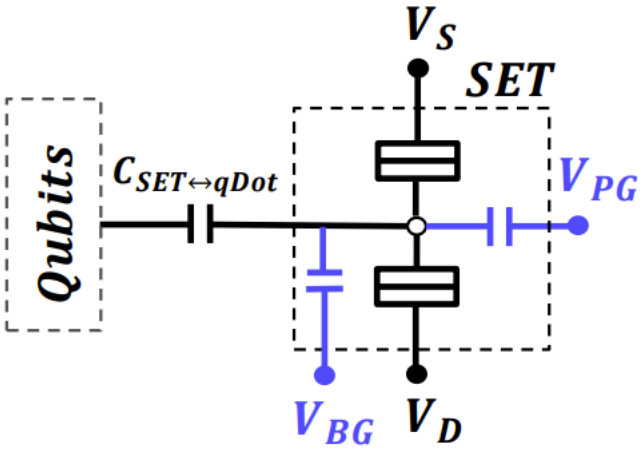

Figure 4 Simplified schematic of a capacitive coupling between SET and qubits. Any tunneling event happening through the quantum dots hosting spin qubits is sensed as a shift in current in the output characteristic of the device.

Exercice 5

The self-capacitance of a metallic grain is sometimes estimated by $C_{self} = V/q$, where V denotes the potential of the grain and q the charge transferred onto it from infinity (at zero potential). For a sphere, C_{self} equals $4\pi\varepsilon r$, whereas, for a circular disk, $C_{self} = 8\varepsilon r$ (r denotes the radius of the island).

a. Estimate C_{self} and the charging energy using both the sphere and circular disk approximations for some reasonable grain radii: 100nm, 10nm and 1nm if the surrounding dielectric is SiO_2 ($\varepsilon_r = 4$).
b. Calculate the radius of metallic grain surrounded by HfO_2 ($\varepsilon_r = 20$) needed to use this grain for a Single Electron Transistor capable to operate at T = 10 K. Recalculate the same for T = 300 K.

Answer:

a. For this exercise we're considering an ideal grain (or island, or quantum dot, …) and its self-capacitance, regardless of the exact structure of the device. For the spherical geometry, the charging energy is $E_C = e^2/C$ (note that there is no "2" at the denominator, which appears in the formula where we consider that the capacitance of the grain comes from the plate capacitors around it). For the disk geometry, we will use the same formula.
   If we calculate the self-capacitance for the two geometries and three diameters, remembering that $\varepsilon = \varepsilon_0\varepsilon_r$, where $\varepsilon_0 = 8.85\text{x}10^{-12}$ $C^2/N\cdot m^2$, we obtain the following values:

	Sphere	Disk
r = 100 nm	44.5 aF	28.3 aF
10 nm	4.45 aF	2.83 aF
1 nm	0.45 aF	0.28 aF

   We can then calculate the charging energy ($e = 1.6\text{x}10^{-19}$ C):

	Sphere	Disk
r = 100 nm	$5.75\text{x}10^{-22}$ J	$9.05\text{x}10^{-22}$ J
10 nm	$5.75\text{x}10^{-21}$ J	$9.05\text{x}10^{-21}$ J
1 nm	$5.75\text{x}10^{-20}$ J	$9.05\text{x}10^{-20}$ J

b. Using the same formulas, we have just to start from the charging energy and obtain the grain diameter (assume to be a sphere), remembering that the dielectric material has changed. The value of the charging energy comes from the restriction of the operating temperature. We can take the ratio $E_C/k_BT = 10$, which is the less restrictive condition (for memory operation), where $k_B = 1.38\text{x}10^{-23}$ J/K. For T = 10 K, we have $E_C = 10\text{x}k_B\text{x}10 = 1.38\text{x}10^{-21}$ J and $r = e^2/4\pi\varepsilon_0\varepsilon_r E_C = 8.34$ nm.
   In the same way, for T = 300 K, r = 2.78 Å.

Exercice 6: Single Electron Transistors - T or F

The SET is a discrete charge device using three conductive nanodots as source, drain and gate and with thin tunneling oxides between central island and the source and the drain, operating under the orthodox theory of Coulomb blockade. Choose the correct properties of this family of devices:

1. A SET inverter can be built with two identical SETs, in contrast with a CMOS inverter that needs one n-type and one p-type MOSFET. This is because a SET shows both positive and negative transconductance, depending on the applied gate voltage.

> **True**: for the same V_{DS}, we can apply a different V_{GS} and operate the device on the left side (positive transconductance $g_m = \partial I_{DS}/\partial V_{GS}$) or the right side (negative transconductance of the same oscillation (= same number of electrons in the dot). Note that, in the inverter depicted in slide 85, V_{in} is the same for the gate capacitor of the two devices, but V_{GS} is the difference between V_{in} and V_{source}, which instead is different in the two devices.

2. SET logic is a wireless logic.

> **False**: logic circuits are built with cables.

3. The I_d-V_d output characteristic of a SET transistor saturates because of the Coulomb blockade effect.

> **False**: at high $|VDS|$, a SET behaves like a resistor.

4. The effect of background charge on a SET affects the values of its threshold voltages.

> **True**: the SET is very sensitive to background charge, which can modify the potential applied to the gate. A small variation in V_{GS} will result in big variations of I_{DS}, because of the steepness of the oscillations (high transconductance).

5. The PADOX technology for SETs uses metal (like Al) dots and SiO_2 as a tunneling dielectric.

> **False**: the PADOX technology is based on Si and SiO_2.

6. With a metallic central island of around 2 nm in diameter, one can obtain a Coulomb blockade effective at room temperature (T=300K).

> **False**: we've seen in the previous exercise that an island one order of magnitude smaller is required.

7. A SET inverter consumes static power in logic 1 and logic 0 states which is contrary to the behavior of a CMOS inverter.

> **True** (see slide 85): in both states, the static current is very low, especially at low temperature.

8. The SET can be used as an ultra-high sensitive elementary charge detector.

True: because of the high charge sensitivity of the gate

9. In a SETMOS hybrid device the period of the oscillations is independent of the amplification of the current provided by the MOSFET device.

True: the intensity of the current is dependent on the MOSFET amplification, but the periodicity of the oscillations is only determined by the SET characteristics (slide 101).

10. The intrinsic frequency operation (speed) of SETs is limited to kHZ to MHz range due to their very low currents (typically less than nA).

False: in principle, the smaller capacitances in the device allow even higher frequency.